# High-Speed Signal Testing Solutions



SOLUTIONS
PSO2407-0007EN01

SIGLENT TECHNOLOGIES CO.,LTD

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#### **Product Certification**

SIGLENT certifies that this product complies with China's national product standards and industry product standards, and further certifies that this product complies with the relevant standards of other members of international standards organizations.

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# **№** 1 OVERVIEW

With the rapid development of electronic technology, the speed of information exchange continues to increase, and the frequency and complexity of high-speed signals are also constantly rising. Accurately testing and measuring high-speed signals is crucial for ensuring the normal operation of various systems. What kind of signal can be called a high-speed signal? We typically consider signals with the following characteristics as high-speed signals:

- Signals with frequencies greater than 50 MHz, especially clock signals reaching frequencies above 50 MHz.
- Fast-edge signals with short rise times. When the rise time is less than 50 ps, the signal transition speed is extremely fast and can also be classified as a high-speed signal.
- From the perspective of trace length, if the trace length is less than 20% of the effective wavelength
  and the signal has a short rise time, it also falls within the category of high-speed signals.

## 2 CHALLENGES

High-speed signals possess distinct characteristics. They are susceptible to various interferences during transmission, such as electromagnetic interference (EMI) and crosstalk, which can lead to signal distortion. Furthermore, the high frequency of high-speed signals often demands that components within the circuit respond quickly to ensure accurate signal transmission.

## 3 SOLUTION

Signal integrity (SI) refers to the fidelity of a signal during transmission. It primarily studies the degradation of signal quality in high-speed signals caused by factors such as impedance matching and crosstalk. It characterizes the quality issues arising in high-speed signals after traversing a link due to interference and impedance factors within the link, thereby ensuring reliable transmission between the transmitter and receiver.

Signal integrity testing encompasses a wide range of content and utilizes diverse test instruments. Next, we will introduce several common testing methods to help engineers quickly locate and resolve issues.

## 3.1 Waveform Testing

Waveform testing is the simplest and most common method in signal integrity testing. By observing the amplitude, edge characteristics, overshoot, undershoot, etc., of the waveform captured by an oscilloscope, one can determine whether the signal still meets the receiver's level requirements after passing through the transmission link.

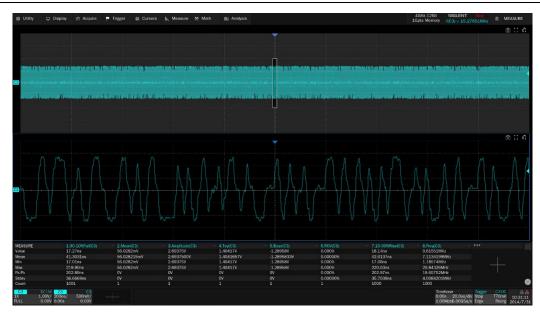


Figure 3.1 Testing Ethernet Signal Using SDS7000A

After the oscilloscope captures the waveform, the waveform can be zoomed in. This allows us to observe the overall waveform characteristics via the statistics bar below the oscilloscope display and also examine local details such as the amplitude of overshoot and undershoot.

When observing certain digital signals, timing is a critical concern. We can use an 8-channel oscilloscope to help observe the setup and hold times of individual signals, measure the skew and delay introduced by circuit networks on different signals, or analyze power rail sequencing in embedded circuits using specific triggers to verify the power-up/power-down timing requirements at different nodes.

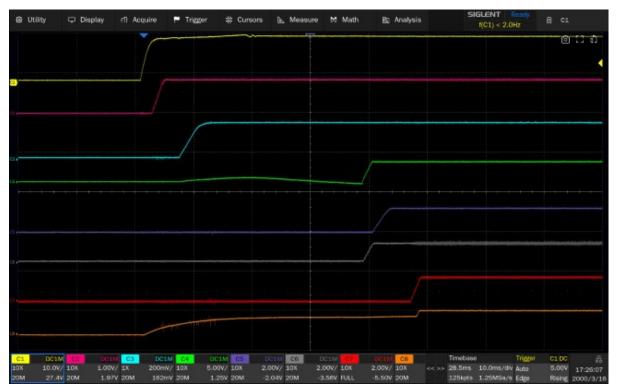


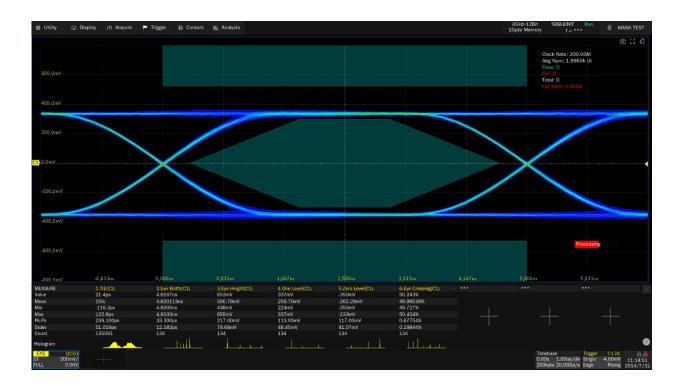
Figure 3.2 Power-Up Sequence Analysis Using 8 Channels

## 3.2 Eye Diagram Testing

The eye diagram of a digital signal contains rich information, reflecting the overall characteristics of the signal and providing an excellent assessment of its quality. Therefore, eye diagram analysis is a cornerstone of signal integrity analysis in digital systems. Especially for interfaces with specific compliance standards, such as USB, Ethernet, PCIe, HDMI, etc., eye diagram testing combined with masks can verify whether the interface meets the consistency specifications.

An Eye Diagram is the result of accumulatively overlaying captured bits of a serial signal using a persistence display mode. The resulting superimposed pattern resembles an eye, hence the name. It graphically represents a series of digital signals accumulated on an oscilloscope. It contains abundant information; the effects of inter-symbol interference (ISI) and noise can be observed from the eye diagram, revealing the overall characteristics of the digital signal and allowing an estimation of system performance.

SIGLENT's SDS7000A Real-Time Eye Diagram feature can automatically generate the eye diagram of a signal. After specifying the signal source, clicking "Quick Setup" in the UI automatically configures the horizontal/vertical scales and threshold levels, and calls up common measurement parameters such as Eye Height, Eye Width, and Time Interval Error (TIE).



## 3.3 Jitter Analysis

As data rates continue to increase, the timing margin in high-speed digital circuit design becomes

increasingly smaller. To ensure that serial data signals captured at the receiver are valid and stable, engineers need to be familiar with various jitter components, especially their impact on the data valid window. Currently, oscilloscopes are primarily used to capture and analyze waveform jitter. The SDS7000A offers a jitter analysis measurement option, displaying jitter in various ways and decomposing different jitter components.

Jitter refers to the deviation of a timing signal from its ideal position over time, often called Time Interval Error (TIE). It involves statistical analysis of the cumulative time value deviation of each cycle point relative to its ideal value at the current time point. This time deviation algorithm exhibits a cumulative effect (an integration operation), reflecting the signal's long-term jitter. Most modern high-speed serial buses use embedded clocks. Embedded clocks must be recovered by the receiver before analysis can be performed. Performing jitter analysis on serial bus data signals containing embedded clocks requires the oscilloscope to recover the clock from the data signal. The software algorithm within the jitter analysis option accomplishes this by creating a virtual clock to emulate the clock recovery process at the serial data bus receiver. Using this recovered clock as a reference, the oscilloscope aligns each edge of the serial data captured in its memory to perform TIE measurements.

In practice, eye diagram and jitter analysis are often discussed together because their analysis methodologies are similar: both involve clock recovery first, followed by waveform analysis using the recovered clock as a reference. Their difference lies in the fact that an oscilloscope's eye diagram typically only analyzes total jitter (TIE), whereas the dedicated jitter analysis function can decompose the total jitter into different components (such as RJ - Random Jitter, DCD - Duty Cycle Distortion, PJ - Periodic Jitter), enabling better signal analysis.

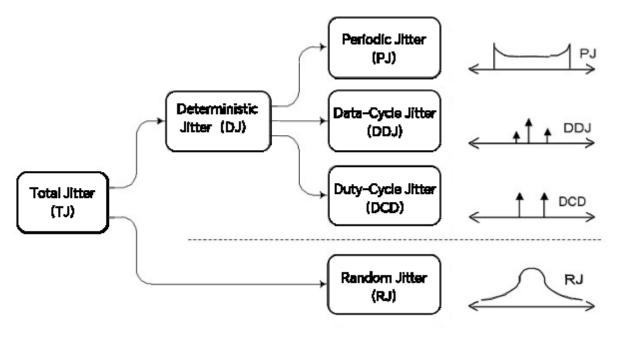


Figure 3.3 Jitter Decomposition



Figure 3.4 Jitter Analysis Using SDS7000A

## 3.4 Impedance Testing

For high-speed signals, impedance matching is a critical concern. Impedance mismatches cause reflections that generate noise at the receiver. Therefore, Vector Network Analyzers (VNAs) are commonly used for impedance analysis to characterize noise caused by multiple reflections.

For traces on PCBs, a VNA paired with a TDR (Time Domain Reflectometry) probe can also be used for testing. Compared to the TDR solution using an oscilloscope + signal generator, a VNA enables testing at higher frequencies and offers more flexibility in signal injection methods (e.g., probe selection).

Impedance mismatch, especially in differential circuits, significantly impacts signal quality. The figure below shows the same DUT transmitting a PAM3 differential signal. The pink trace represents the signal received when the two differential lines are well matched. The yellow trace shows the signal under imperfect matching. It is evident that the yellow trace exhibits significant overshoot and undershoot.

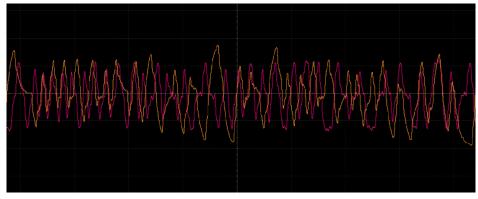


Figure 3.5 Signal Quality on Differential Lines Under Different Matching Conditions

When testing differential impedance, the TDR function of a network analyzer can be used to test singleended trace impedance or directly measure differential impedance.



Figure 3.6 Testing Using a TDR Probe

# 3.5 Frequency Domain Testing

When high-speed signals propagate along conductors on a PCB, they essentially travel as electromagnetic waves. Energy exists within alternating electric and magnetic fields along the entire transmission path. In practical applications, electromagnetic field energy is not confined solely to the propagating conductor; a significant portion of the magnetic field energy exists outside the conductor. When a high-speed signal travels along one conductor, its electric and magnetic fields can couple into other lines through various mechanisms. When the intensity of this coupled electromagnetic field reaches a certain level, it generates unintended signals, leading to crosstalk and electromagnetic radiation, which can severely impact the transmission quality of the original signal.

Vector Network Analyzers (VNAs) can be used to perform crosstalk testing on signal links. Limits can be set before testing begins to enable automated testing. Near-end crosstalk (NEXT) is a key consideration when PCB traces are long or data rates are very high. For testing differential signals, a four-port VNA can be used directly, or a balun can be employed to convert the signal to single-ended for testing.

During later system testing phases (such as EMC testing), many products require radiated emissions testing. Spectrum analysis can identify whether power levels at certain frequencies exceed limits. Near-field probes, such as the SRF5030 series, can be used to pinpoint which specific areas on a board card exhibit higher spectral emissions, helping to locate the root cause of non-compliance.



Figure 3.7 EMI Testing Using a Spectrum Analyzer

Advantages of frequency domain testing include:

- Providing an intuitive display of signal distribution across different frequencies.
- Facilitating convenient measurement and analysis of system frequency response characteristics, such as bandwidth and gain flatness.
- For some complex signals or systems, frequency domain analysis may reveal issues more readily
  than time domain analysis. In high-speed signal testing, time domain and frequency domain
  analyses are often combined to provide a more comprehensive understanding and evaluation of
  overall system performance.

# Products Mentioned in This Document

Name	Model	Description
Oscilloscope	SDS6000A	Oscilloscopes equipped with
	SDS7000A	jitter and eye diagram analysis capabilities
Differential Probe	SAP2500D	2.5GHz and 5GHz Active
	SAP5000D	Differential Probes
Vector Network Analyzer	SNA5000X	Vector Network Analyzers
	SNA6000A	equipped with TDR functionality
TDR Probe	ASP-26	Used with VNAs to expand
	ADP-26	application scenarios
Spectrum Analyzer	SSA3000X plus	Used as receivers for EMC

	SVA1000X	testing
Near-Field Probe	SRF5030	For radiation testing
	SRF5030T	



#### About SIGLENT

SIGLENT is an international high-tech company, concentrating on R&D, sales, production and services of electronic test & measurement instruments.

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SIGLENT first began developing digital oscilloscopes independently in 2002. After more than a decade of continuous development, SIGLENT has extended its product line to include digital oscilloscopes, isolated handheld oscilloscopes, function/arbitrary waveform generators, RF/MW signal generators, spectrum analyzers, vector network analyzers, digital multimeters, DC power supplies, electronic loads and other general purpose test instrumentation. Since its first oscilloscope was launched in 2005, SIGLENT has become the fastest growing manufacturer of digital oscilloscopes. We firmly believe that today SIGLENT is the best value in electronic test & measurement.

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